CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a set of voltage generators to generate a set of direct current (DC) voltages;

a set of sense amplifiers coupled to compare a reference voltage with the set of DC voltages; and

logic coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the reference voltage and the set of DC voltages.

2. The integrated circuit of claim 1 wherein the set of voltage generators is responsive to a set of configuration bits to determine the set of DC voltages.

3. The integrated circuit of claim 2, further comprising a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers.

4. The integrated circuit of claim 2, wherein each voltage generator in the set of voltage generators is a digital-to-analog converter.

5. The integrated circuit of claim 1, further comprising second logic coupled to open and close the set of switches to connect the set of DC voltages to the non-inverting inputs of the set of sense amplifiers.

6. The integrated circuit of claim 5, wherein the second logic comprises a boundary-scan register.

7. The integrated circuit of claim 5, wherein the second logic comprises an input/output loop back pattern generator.

8. A system, comprising:

an integrated circuit having a set of voltage generators to generate a set of direct current (DC) voltages, a set of sense amplifiers coupled to compare a reference voltage with the set of DC voltages, and logic coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the reference voltage and the set of DC voltages; and

a structural tester coupled to the integrated circuit to apply a reference voltage to the inverting input of each sense amplifier in the set of sense amplifiers.

9. The system of claim 8, wherein the set of voltage generators is responsive to a set of configuration bits to determine the set of DC voltages.

10. The system of claim 8, wherein the integrated circuit further comprises a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers.

11. The system of claim 8, wherein each voltage generator in the set of voltage generators is a digital-to-analog converter.

12. The system of claim 8, wherein the logic to interpret the comparison of the reference voltage and the set of analog voltages comprises a boundary scan register.

13. The system of claim 8, wherein the logic to interpret the comparison of the reference voltage and the set of analog voltages comprises input/output loop back compare circuitry.

14. The system of claim 8, wherein the integrated circuit further comprises a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers, and wherein the integrated circuit further comprises second logic coupled to open and close the set of switches.

15. The system of claim 14, wherein the second logic comprises a boundary-scan register.

16. The system of claim 14, wherein the second logic comprises an input/output loop back pattern generator.

17. A method of manufacturing an integrated circuit, comprising:

coupling a set of levels generating circuits to a set of sense amplifiers, wherein the set of sense amplifiers are to compare a reference voltage to a set of direct current (DC) voltage levels generated by the set of levels generating circuits; and

coupling the set of sense amplifiers to logic to interpret the comparison of the reference voltage and the set of voltage levels.

18. The method of claim 17, further comprising coupling the set of levels generating circuits to be responsive to a set of configuration bits to set the values of the set of DC voltage levels.

19. The method of claim 18, further comprising coupling a set of switches between the set of levels generating circuits and the set of sense amplifiers to enable the set of DC voltage levels to be applied to the non-inverting input of each sense amplifier.

20. The method of claim 19, wherein coupling a set of levels generating circuits to a set of sense amplifiers comprises coupling a set of digital-to-analog converters to the set of sense amplifiers.

21. The method of claim 17, wherein coupling the set of sense amplifiers to logic to interpret the comparison of the reference voltage and the set of DC voltage levels comprises coupling the set of sense amplifiers to a boundary scan register to interpret the comparison of the reference voltage and the set of DC voltage levels.

22. The method of claim 17, wherein coupling the set of sense amplifiers to logic to interpret the comparison of the reference voltage and the set of DC voltage levels comprises coupling the set of sense amplifiers to input/output loop back compare circuitry to interpret the comparison of the reference voltage and the set of DC voltage levels.

23. The method of claim 19, further comprising coupling second logic to open and close the set of switches.

24. The method of claim 23, wherein coupling second logic to open and close the set of switches comprises applying values from a boundary-scan register to open and close the set of switches.

25. The method of claim 23, wherein coupling second logic to open and close the set of switches comprises applying values from an input/output loop back pattern generator to open and close the set of switches, wherein the second logic comprises an input/output loop back pattern generator.

26. An apparatus, comprising:

an integrated circuit device having:

a first number of input pins; and

levels generating circuitry coupled to at least some of the first number of input pins, the levels generating circuitry being responsive to a set of configuration bits to enable concurrent input levels testing or parallel input levels testing of the first number of input pins using a second smaller number of input pins.

27. The apparatus of claim 26, wherein the levels generating circuitry comprises:

a set of voltage generators to generate a set of direct current (DC) voltages;

a set of sense amplifiers coupled to compare a reference voltage with the set of DC voltages; and

logic coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the reference voltage and the set of DC voltages.

28. The apparatus of claim 27, further comprising a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers.

29. The integrated circuit of claim 27, wherein each voltage generator in the set of voltage generators is a digital-to-analog converter.

30. A method, comprising:

testing at least one integrated circuit device having a first number of input pins and levels generating circuitry coupled to at least some of the first number of input pins by:

receiving a set of configuration bits at the levels generating circuitry; and

receiving test input levels at a second smaller number of input pins to enable parallel input levels testing of the first number of input pins.

31. The method of claim 30, further comprising:

generating direct current (DC) voltages;

comparing a reference voltage with the set of DC voltages; and

interpreting the comparison of the reference voltage and the set of DC voltages.

32. The method of claim 31, wherein receiving a set of configuration bits at a levels generating circuitry comprises receiving a set of configuration bits at digital-to-analog converters.